(SM)

Notice of Allowability	Application No.	Applicant(s)	
	10/643,955	CHEN, CHUN-YING	
	Examiner	Art Unit	
	Gary L. Laxton	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the application filed 8/20/03*.

2. ☒ The allowed claim(s) is/are *1-8*.

3. ☒ The drawings filed on *20 August 2003* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

1/24/05

Gary L. Laxton
Patent Examiner
Art Unit: 2838

DETAILED ACTION

Allowable Subject Matter

1. Claims 1-8 are allowed.

2. The following is an examiner's statement of reasons for allowance:

Claims 1-3; prior art fails to disclose or suggest, inter alia, a power supply multiplexing circuit comprising a first supply voltage input; a first pair of cascoded PMOS transistors in series with the first supply voltage input; a first native NMOS transistor in series with the fist pair of cascoded PMOS transistors; a second supply voltage input; a second pair of cascoded PMOS transistors in series with the second supply voltage input; and a second native NMOS transistor in series with the second pair of cascoded PMOS transistors, wherein the gates of the first and second native NMOS transistors are driven by two control signals out of phase with each other, and wherein sources of the first and second native NMOS transistors are connected together to output an output voltage.

Claims 4 and 5; prior art fails to disclose or suggest, inter alia, a power supply multiplexing circuit comprising two half-cells, each half cell including; a first supply voltage input; in series, a first cascoded PMOS transistor connected to a corresponding supply voltage, a second cascoded PMOS transistor, and a native NMOS transistor; wherein the gates of the native NMOS transistors are driven by two control signals out of phase with each other, and wherein sources of the first and second native NMOS transistors are connected together to output an output voltage.

Claims 6-8; prior art fails to disclose or suggest, inter alia, a power supply multiplexing circuit comprising a first pair of PMOS transistors in series with a first voltage input, a first native NMOS transistor in series with the first pair of PMOS transistors; a second pair of PMOS transistors in series with a second voltage input; and a second native NMOS transistor in series with the second pair of PMOS transistors, wherein the gates of the first and second native NMOS transistors are driven by two control signals out of phase with each other, and wherein sources of the first and second native NMOS transistors are connected together.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US 6,049,227 Goetting et al discloses an FPGA with a plurality of input voltage levels.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary L. Laxton whose telephone number is (571) 272-2079. The examiner can normally be reached on Monday thru Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on (571) 272-2084. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

1/24/05

Gary L. Laxton
Patent Examiner
Art Unit 2838